PRN:		Course Code :	ECE403R1

Final Year **B. Tech** End Semester Examination Winter 2023

VLSI System Design

Day and Date: Thursday, 30/11/2023 **Max Marks:** **100**

Time : 2.00 to 5.00 pm **Duration:** **03** hrs

Instructions:All questions are compulsory.

			Marks	Bloom's Level	CO
Q.1		**Attempt the following**			
	a)	With neat and suitable block diagram, explain VLSI design flow.	08	2	1
	b)	What is the need of HDL? Explain different features of VHDL.	08	2	1
		OR			
	b)	Explain briefly the different levels of abstraction.	08	2	1
Q.2		**Attempt the following**			
	a)	Write a VHDL code to realize 1:4 Demultiplexer	08	6	2
	b)	Write a VHDL code to realize JK-FlipFlop.	08	6	2
		OR			
	b)	Draw the full adder circuit using two half adder circuits. Write a VHDL code for full adder using 'Process' statement.	08	6	2
Q.3		**Attempt any two from the following**			
	a)	What is meant by "Drain punch through?"	08	2	3
	b)	Explain Noise Margin of CMOS Inverter	08	2	3
	c)	Draw and explain the voltage transfer characteristics of CMOS inverter.	08	2	3
Q.4		**Attempt any two from the following**			
	a)	State CMOS design methodology and design CMOS inverter (NOT) gate.	08	2	3
	b)	Design of XOR Gate- as Boolean expression given as $Y = A\overline{B} + \overline{A}B$	08	6	2
	c)	Design Half adder circuits (CMOS Technology)	08	6	2

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Q.5	**Attempt any Two of the following**				
	a)	Write a Verilog code to realize Binary to Gray and Gray to Binary Code conversion	09	6	2
	b)	Explain Verilog operators.	09	6	2
	c)	Explain Net and Register data type in Verilog	09	3	2
Q.6	**Attempt any Two of the following**				
	a)	Explain Spartan-III FPGA (XC3S400) architecture.	09	2	1
	b)	State different FPGA Programming Technologies and explain any one.	09	2	3
	c)	Write a note on Built-In Self-Test (BIST) Techniques	09	2	3

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